What is claimed is:

1. A feedback control I/O buffer driven by a system voltage, comprising:

an input/output circuit comprising a first PMOS transistor and a first NMOS transistor and having an I/O port coupled to an I/O pad, wherein the first PMOS transistor has an N-well region, a gate of the first NMOS transistor receives a first gate control signal, and a drain of the first PMOS transistor serves as the I/O port;

a N-well control circuit coupled to I/O pad to control the voltage level at the N-well region of the first PMOS transistor according to the feedback signal output from the inverter; and

a P-gate control circuit receiving a second gate control signal and being output to the gate of the first PMOS transistor, wherein the P-gate control circuit comprises:

a transmission gate having a second NMOS transistor and a second PMOS transistor, the sources of which are coupled to the second gate control signal, and the gates of which are coupled to the system voltage and the N-well control circuit respectively; and

a third PMOS transistor having a drain and a source coupled to the gate and the floating N-well region of the first PMOS transistor respectively, and a gate coupled to the system voltage.

2. The feedback control I/O buffer as claimed in Claim 1, wherein the N-well control circuit adjusts the voltage level at the N-well region of the first PMOS transistor to the voltage level of the input voltage when the input voltage exceeds the system voltage.

3. The feedback control I/O buffer as claimed in Claim 2, wherein the N-well control circuit adjusts the voltage level at the N-well region of the first PMOS transistor to the voltage level of the system voltage when the input voltage is lower than the system voltage.

4. The feedback control I/O buffer as claimed in Claim 1, wherein the input/output circuit further comprises a fourth NMOS transistor having a source and drain coupled to the I/O pad and the drain of the first NMOS transistor respectively, and a gate coupled to the system voltage.

5. The feedback control I/O buffer as claimed in Claim 4, wherein the N-well control circuit comprises:

a fourth PMOS transistor having a source coupled to the I/O pad, a gate coupled to the system voltage, and a drain coupled to the N-well region of the first PMOS transistor;

a fifth PMOS transistor having a gate coupled to the system voltage, a source coupled to the I/O pad, and a drain;

a sixth PMOS transistor having a gate coupled to the drain of the fifth PMOS transistor, a drain coupled to the system voltage, and a source coupled to the N-well region of the first PMOS transistor; and

a fourth NMOS transistor having a source and drain coupled to the I/O pad and the gate of the sixth PMOS transistor, and a gate coupled to the system voltage.

6. An input/output buffer, comprising:

a floating N-well;

a first NMOS transistor having a gate coupled to a first gate control signal, and a source coupled to the ground;

a second NMOS transistor having gate coupled to a system voltage, a source coupled to a drain of the first NMOS transistor and a drain coupled to an I/O pad;

a third NMOS transistor having a gate coupled to the system voltage, and a drain coupled to the I/O pad;

a first PMOS transistor having a source coupled to the system voltage, and a drain coupled to I/O pad;

a second PMOS transistor having a source coupled to the I/O pad, a gate coupled to the system voltage, and a drain coupled to floating N-well;

a third PMOS transistor having a source coupled to I/O pad, a gate coupled to the system voltage, and a drain coupled to a source of the third NMOS transistor;

a fourth PMOS transistor having a gate coupled the drain of the third PMOS transistor, a drain coupled to the system voltage, and a source coupled to the floating N-well;

a transmission gate including a fifth PMOS transistor and a fourth NMOS transistor, wherein the sources

of which are coupled to a second gate control signal, the drains of which are coupled to the gate of the first PMOS transistor, and the gates of which are coupled to a drain of the third PMOS transistor and the system voltage respectively; and

a sixth PMOS transistor having a gate coupled to the system voltage, a drain coupled to the gate of the first PMOS transistor and a source coupled to the floating N-well and the source of the fourth PMOS transistor; wherein the floating N-well is connected to the substrate on which the first to sixth PMOS transistors are formed.